What is Claimed is:

[c1] A semiconductor device comprising:
a fin body, the fin body having a sidewall;
a gate insulator formed on the fin body sidewall;
at least one floating gate formed on the gate insulator, the at least one floating gate having an exterior side;
a floating gate insulator formed on the floating gate exterior side; and
a control gate formed on the floating gate insulator, the floating gate isolated from the control gate by the floating gate insulator.

[c2] The semiconductor device of Claim 1 wherein the semiconductor device comprises an NVRAM memory cell.

[c3] The semiconductor device of Claim 1 wherein said at least one floating gate comprises a spacer.

[c4] The semiconductor device of Claim 1 wherein the at least one floating gate comprises a double floating gate.

[c5] The semiconductor device of Claim 4 wherein each floating gate of said double floating gates is isolated from the other.

[c6] The semiconductor device of Claim 4 wherein each floating gate of said double floating gate is electrically connected to the other.

[c7] The semiconductor device of Claim 1 wherein said fin body is sufficiently thin to provide full depletion when the device is in operation.

[c8] The semiconductor device of Claim 1, wherein said fin body sidewall comprises a source/drain region and wherein each source/drain region is surrounded by insulation on at least three sides.

[c9] The semiconductor device of Claim 8 wherein the source/drain regions are surrounded by insulation on four sides.

[c10] The semiconductor device of Claim 1 wherein the semiconductor device is configured for horizontal current flow.

[c11] An NVRAM device comprising:
a transistor body having two sides;
a gate insulator disposed on both of said sides of the transistor body; and,
First and second floating gates disposed on the gate insulator each being disposed on a respective side of said transister body, wherein said first and second floating gates store a memory signal for the NVRAM device.

[c12] The NVRAM device of claim 11 wherein the transistor body is a fin body.

[c13] The NVRAM device of claim 11 further comprising a control gate formed over said first and second floating gates.

[c14] The NVRAM device of claim 11 wherein said first and second floating gates isolated from the other.

[c15] The NVRAM device of claim 11 wherein said first and second floating gates are electrically connected to the other.

[c16] The NVRAM device of claim 11 wherein the device is configured for horizontal current flow.

[c17] A method of fabricating a semiconductor device comprising the steps of:
forming a fin on a semiconductor wafer;
providing a first dielectric on said fin;
depositing a first conductive material for a floating gate on said first dielectric;
providing an insulator layer on said first conductive material;
depositing a second layer of conductive material for a control gate on said insulator layer; and
patterning said second layer of conductive material and said first conductive material.

[c18] The method of Claim 18 further comprising in step (c) the step of spacer etching said first conductive material to form a spacer floating gate.

[c19] The method of Claim 18 further comprising in step (c) the step of spacer etching said first conductive material to form a double spacer floating gate.

[c20] The method of Claim 18 wherein step (a) further comprises the step of forming a hard mask material on top of said fin to protect said fin where it extends beyond said second conductive material.